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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,354	07/07/2003	Thomas J. Sonderman	2000.100800	7900

23720 7590 12/28/2005

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EXAMINER
NGUYEN, KHIEM D

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 12/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	10/614,354	SONDERMAN ET AL.	
	Examiner	Art Unit	
	Khiem D. Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,6-9,11-15,21 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,6-9,11-15,21 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Applicants' Arguments

The final rejection as set forth in paper No. (061505) mailed on June 21st, 2005 is withdrawn in response to Applicants' arguments on October 11th, 2005. A new non-final rejection is made as set forth in this Office Action. Claims (1, 3, 6-9, 11-15, 21 and 22) are pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 6-9, 11-15, and 21-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Fang et al. (U.S. Patent 6,133,746).

In re claims 1 and 9, **Fang** discloses a method, comprising: performing at least one electrical test **102** on at least one flash memory device (col. 1, lines 35-48) to determine a duration of a programming cycle **104** performed on the flash memory device; determining at least one parameter **106** of at least one process operation to be performed to form at least one gate insulation layer **108** on a subsequently formed flash memory device based upon the determined duration of the programming cycle (col. 3, line 66 to col. 4, line 35 and FIG. 1); and

performing the at least one process operation comprised of the determined at least one parameter to form at least one gate insulation layer **108** on the subsequently formed flash memory device (col. 4, line 36 to col. 5, line 21 and FIG. 1).

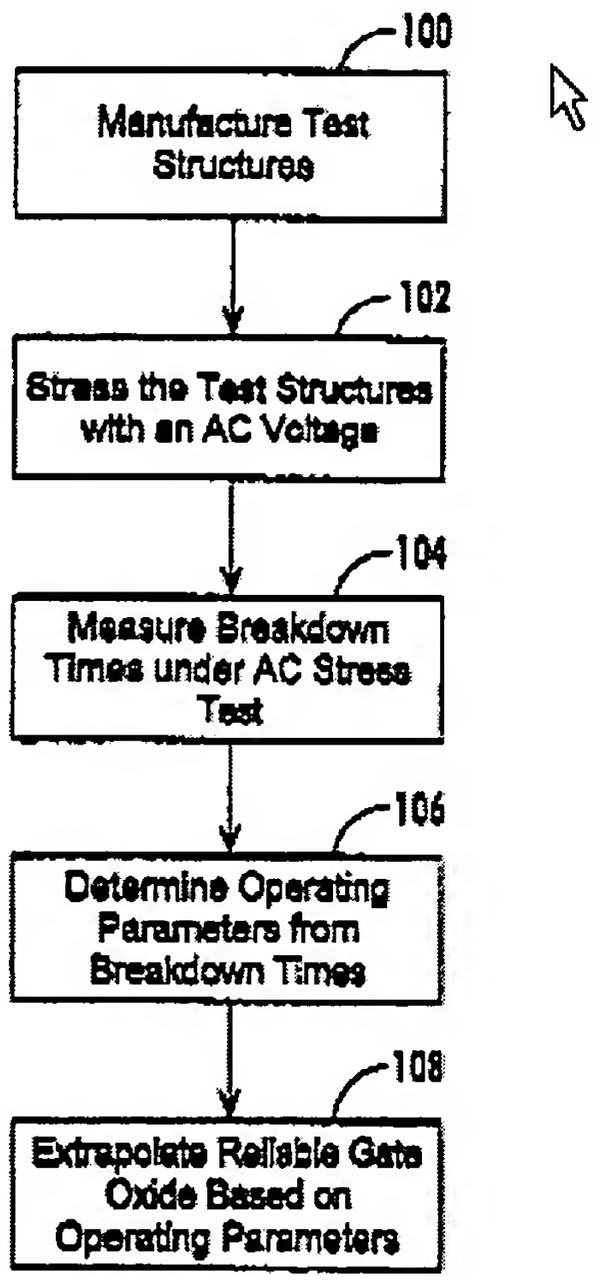

FIG. 1

In re claims 3 and 11, **Fang** discloses that performing the at least one electrical test on the at least one flash device further comprises performing the at least one electrical test on the at least one flash memory device to determine at least one of a breakdown voltage, a threshold voltage, a state charge, an interface charge, a trapped charge, a surface charge, and an erase cycle time (col. 3, line 66 to col. 4, line 35).

In re claims 6 and 13, the technique of performing the at least one process operation comprised at least one of a deposition process and a thermal growth process to form the at least one gate insulation layer on the subsequently formed semiconductor device using a new thickness recipe upon obtaining a new parameter is well-known to one of ordinary skill in the art at the time of the invention was made.

In re claims 7 and 14, **Fang** discloses that at least one parameter is comprised of at least one of a temperature, a pressure, a duration, a process gas flow rate, a process gas composition, a liquid flow rate, a liquid composition, and a power level setting (col. 3, line 66 to col. 4, line 35).

In re claims 8 and 15, **Fang** discloses that the gate insulation layer is comprised of at least one of silicon dioxide and silicon nitride (col. 5, lines 10-21).

In re claim 12, **Fang** discloses that the semiconductor device is comprised of a memory device that is comprised of a gate insulation layer, a floating gate layer positioned above the gate insulation layer, an intermediate insulation layer positioned above the floating gate layer, and a control gate layer positioned above the intermediate insulation layer (col. 1, lines 11-21).

In re claims 21 and 22, **Fang** discloses a method, comprising: performing at least one electrical test **102** on at least one memory device (col. 1, lines 35-48) to determine a duration of a programming cycle **104** performed on the memory devices; determining at least one parameter **106** of at least one process operation to be performed to form at least one gate insulation layer **108** on a subsequently formed memory device based upon the

determined duration of the programming cycle (col. 3, line 66 to col. 4, line 35 and FIG. 1); and

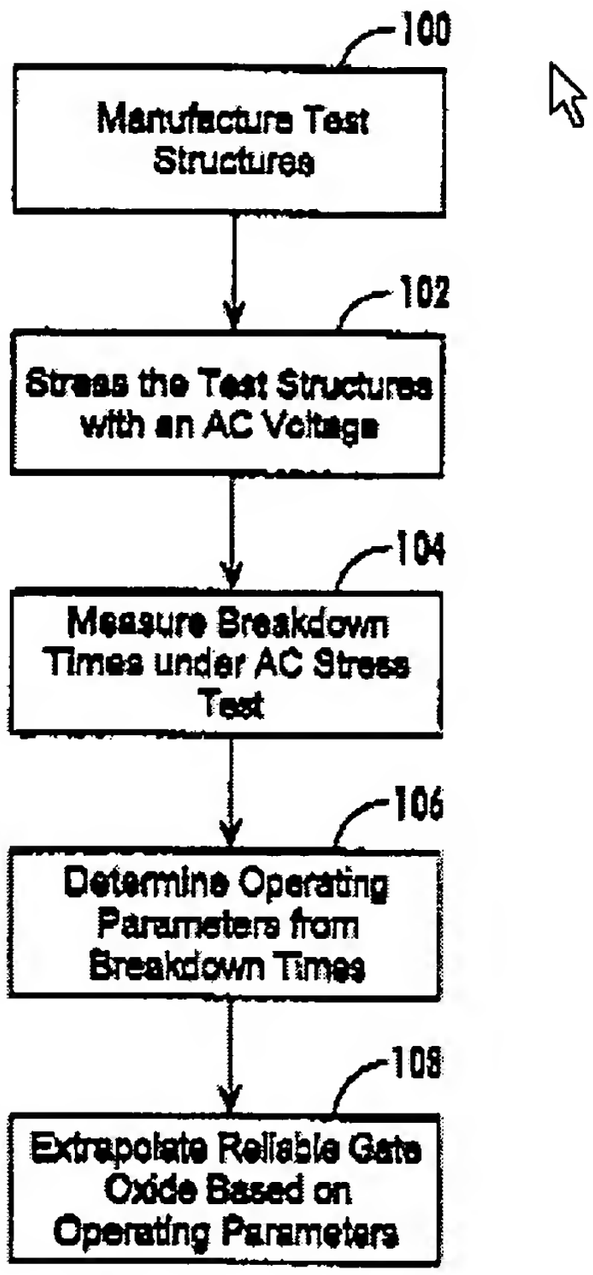

FIG. 1

performing the at least one process operation comprised of the determined at least one parameter to form **108** at least one gate insulation layer on the subsequently formed memory device (col. 4, line 35 to col. 5, line 21).

Response to Applicants' Amendment and Arguments

Applicants contend that at no point does the reference Cappelletti et al. (U.S. Patent 5,793,675) herein Cappelletti even remotely mention or describe the act of

determining at least one parameter of a process operation to be performed to form a gate insulation layer on a subsequently formed memory device based upon electrical test data.

In response to Applicants' contention that Cappelletti does not mention or describe the act of determining at least one parameter of a process operation to be performed to form a gate insulation layer on a subsequently formed memory device based upon electrical test data, Examiner respectfully submits that Applicants' argument is moot in view of the newly discovered reference to Fang et al. (U.S. Patent 6,133,746) applied under 35 U.S.C. 102(b) rejection presented in this Office Action.

Applicants are directed to (col. 3, line 66 to col. 4, line 35 and FIG. 1) where Fang discloses performing at least one electrical test 102 on at least one flash memory device (col. 1, lines 35-48) to determine a duration of a programming cycle 104 performed on the flash memory device and determining at least one parameter 106 of at least one process operation to be performed to form at least one gate insulation layer 108 on a subsequently formed flash memory device based upon the determined duration of the programming cycle. Thus, the newly discovered reference (Fang et al.) discloses the Applicants' claimed invention.

For this reason, Examiner holds the rejection proper.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
December 26, 2005

Brook Kebede

BROOK KEBEDE
PRIMARY EXAMINER